



V5603OCP

10/100 Fast Ethernet Controller with OCP Interface

Features

- Dual speed CSMA/CD (10 Mbps/100 Mbps) Media Access Controller (MAC) compliant with IEEE 802.3, IEEE 802.3u and IEEE 802.3x standards
- PHY interface is fully compliant to Media Independent Interface (MII)
- Programmable to support GPSI (7-wire) for 10Mbps in half-duplex mode
- Address recognition for broadcast, unicast, promiscuous mode and multicast hashing
- MAC Control Sublayer (MCS) function fully compliant with the IEEE 802.3x Flow Control Standards
- Separate transmit and receive FIFOs to support full-duplex operation on the link
- Multiple packets handling in transmit and receive FIFOs
- Supports retransmission after a collision from the Transmit FIFO
- Automatic internal flushing of the receive FIFO for frames less than slot time bits (512 bits) in length
- Interrupts supported per frame, per buffer and for Transmit and Receive events on programmable basis
- Integrated DMA controller with OCP Master Interface (Basic Signals + Simple Extensions), to achieve faster data transfers to/ from memory
- OCP Slave Interface (Basic Signals) for register configuration and PIO mode data transfer
- Core reusability across different On Chip Buses with the help of standard Bus Wrappers
- OCP bus width can be configurable to 16/32/64
- FIFO width configurable to 512/ 1024-bytes

Functional Overview

The V5603OCP is a complete 10/100 Mbps Ethernet controller. The V5603OCP handles all functions associated with movement of data between a 10/100 Mbps Ethernet Transceiver and memory. It interacts with rest of the blocks in a system as shown in Fig 1: V5603OCP in a Typical System. The V5603OCP, on one side interfaces with a 10/100 Mbps MII compatible Transceiver and on the other side the interface is compliant to OCP. The OCP socket interface makes the core independent of the SoC bus and increases its reuse across different embedded applications by using standard bus wrappers. All operations of the core can be controlled and monitored through a set of control and status registers. The core operates in two different modes: DMA mode and Programmed I/O (PIO) mode.

The V5603OCP implements major blocks like DMA Controller for Transmit and Receive Packet Data Transfers, Transmit and Receive FIFO Controllers, Control/status registers and IEEE802.3 compliant 10/100 Mbps MAC function. The DMA Controller block controls the movement of packet data across the FIFO through the OCP master interface (Basic Signals + Simple Extensions) which is totally synchronous to the master clock. Access to internal registers and PIO mode data transfer are through configuration interface (Basic Signals) which is totally synchronous to the slave clock. Signals required to indicate reset, interrupt are provided as OCP sideband signals. The Core interface signals are shown in Fig 2: V5603OCP Megacell I/O Diagram.

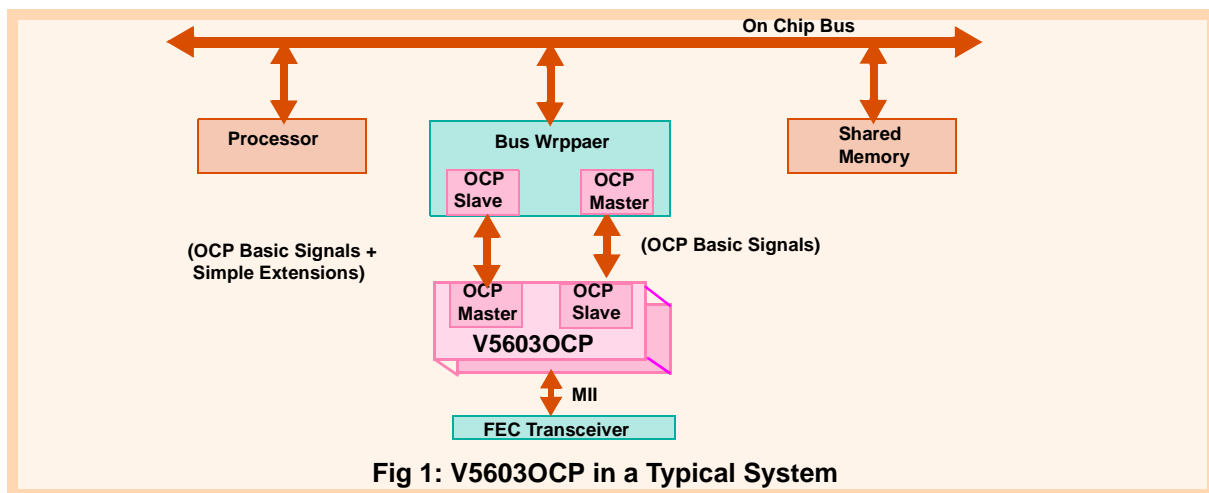


Fig 1: V5603OCP in a Typical System

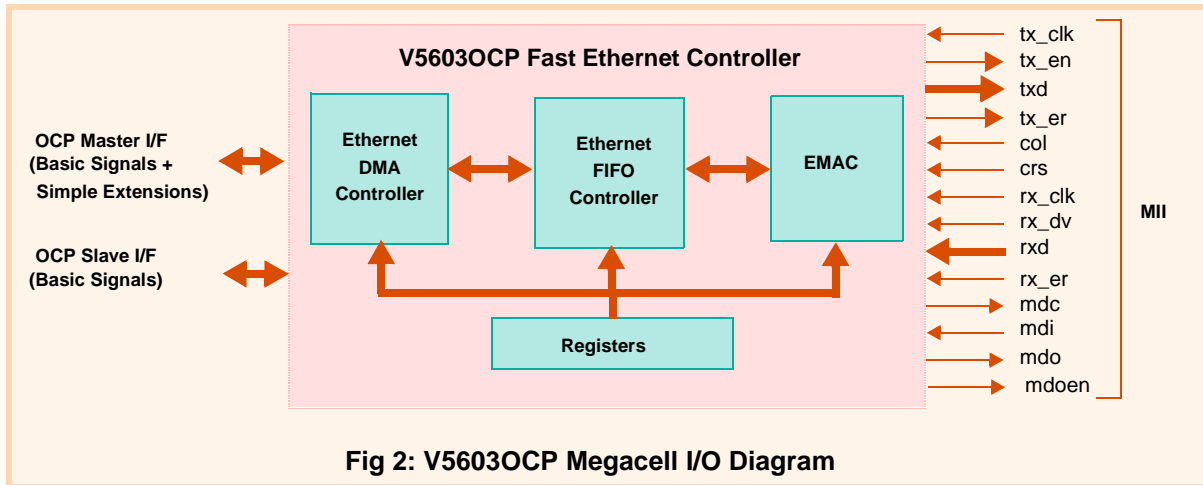


Fig 2: V5603OCP Megacell I/O Diagram

Performance Specifications

Parameter	Value	Remarks
Gate Count	~ 21K ~ 32k	without DMA is 21K with DMA is 32K (The gate count excludes FIFO RAMs)
Code Coverage	100%	Block, ARC, state and transition coverage
OpenMORE Score	95%	
Technology	0.18u	TSMC, Artisan
Frequency	25 - 133MHz	STA verified with pre-route, pre-scan netlist

- Synthesis Scripts
- Scripts for STA & DFT (optional)

Related Products

- V5603, 10/100 FEC with generic interface

Target Applications

- This core intended to use in SoC designs which requires ethernet protocol for media access. Due to the flexibility this core can be integrated into any SoC environment
- It can be used for Ethernet switches, hubs and network interface cards (NICs)

Test Coverage

- Design is highly synchronous and DFT friendly
- Fault coverage is 96% with ATPG vectors

Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data Sheet, User Guide, Verification Description Document
- Self checking Verification Suite

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